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PATENT APPLICATION
DIFFUSION BARRIERS COMPRISING A SELF-ASSEMBLED MONOLAYER

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Diffusion Barriers Comprising Self-Assembled Monolayers

RELATED CASES

[01] This application is related to and claims priority to provisional Applications Nos. 60/240,109 entitled Diffusion Barriers Comprising A Self-Assembled Monolayer naming G. Ramanath, Ahila Krishnamoorthy, Kaushik Chanda and Shyam P. Murarka as inventors and filed October 12, 2000 and 60/244,160 entitled Diffusion Barriers Comprising A Self-Assembled Monolayer naming G. Ramanath, Ahila Krishnamoorthy, Kaushik Chanda and Shyam P. Murarka as inventors and filed October 27, 2000. These applications are incorporated herein for all purposes as if set forth herein in full.

STATEMENT AS TO RIGHTS TO INVENTIONS MADE UNDER FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

[02] NOT APPLICABLE

REFERENCE TO A "SEQUENCE LISTING," A TABLE, OR A COMPUTER PROGRAM LISTING APPENDIX SUBMITTED ON A COMPACT DISK

[03] NOT APPLICABLE

BACKGROUND OF THE INVENTION

A. Field Of The Invention

[04] The present invention generally relates to integrated circuits. In particular, it relates to forming a diffusion barrier layer comprising a self-assembled monolayer in an integrated circuit.

B. Description Of Related Art

[05] Copper is becoming the metal of choice for forming conductive patterns in integrated circuits. There are, however, unresolved issues with its use. For instance, copper diffuses rapidly in silicon and silicon dioxide. The diffusion, over time, results in junction linkage, which decreases device efficiency.

[06] To address the problem of copper diffusion, researchers have developed "diffusion barriers." A diffusion barrier is part of the metallization scheme, comprising a layer of material formed between an overlying copper layer and an underlying

silicon or silicon dioxide layer. The diffusion barrier serves to inhibit the diffusion of copper into the surrounding layer.

[07] The use of amorphous alloys as diffusion layers has been discussed. Amorphous binary silicides, such as molybdenum-, tantalum and tungsten silicide and amorphous ternary alloys (e.g., Ti-Si-N) have been reported as diffusion barriers. The formation of these layers uses sophisticated processes, such as sputtering and/or chemical vapor deposition, or their variants. This results in the inclusion of substantial contaminants and residual stresses. Perhaps more importantly, these films have poor continuity and uniformity in non-planar structures.

[08] Diffusion barriers made of TiN, TiSiN and TiN/TiSiN have also been reported. Many of the processes to form these layers involve treatments such as nitridation, oxidation, and post-deposition annealing.

[09] While a number of diffusion barriers have been discussed in the art, improved diffusion barriers are desirable, especially those that are very thin and continuous.

SUMMARY OF THE INVENTION

[10] The present invention provides a method for forming a diffusion barrier layer. The method involves the following steps: 1) preparing a silicon substrate; 2) contacting the prepared silicon substrate with a composition comprising self-assembled monolayer subunits and a solvent; and, 3) removing the solvent.

[11] The present invention also provides a diffusion barrier in an integrated circuit. The diffusion barrier includes a self-assembled monolayer.

[12] The present invention further provides an integrated circuit with a multilevel metallization scheme. The integrated circuit includes a silicon substrate, a diffusion barrier layer and a metal deposited on the diffusion barrier layer. The diffusion barrier layer is covalently attached to the silicon substrate and includes a self-assembled monolayer.

BRIEF DESCRIPTION OF THE DRAWINGS

[13] FIG. 1 shows a cross-sectional view of an MOS test structure comprising a self-assembled monolayer diffusion barrier layer.

[14] FIG. 2 shows a bar graph representing bias temperature testing of five different test structures.

[15] FIG. 3 shows a cross-sectional view of a two-level integrated circuit comprising a self-assembled monolayer diffusion barrier layer.

DESCRIPTION OF THE SPECIFIC EMBODIMENTS

A. Introduction

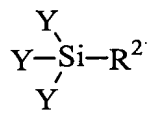
[16] The present invention provides a diffusion barrier in an integrated circuit, a method for forming the diffusion barrier and an integrated circuit containing the diffusion barrier. The diffusion barrier includes a self-assembled monolayer. Formation of the monolayer is typically done on the surface of a silicon substrate by contacting the substrate with monolayer subunits. The silicon substrate is represented by the formula SiO_AX_B, wherein A and B are ≥ 0, and X is N, C, B, F, P or As. In particular, in addition to subscript A assuming particular values of 0, 1, and 2, fractional compositions are also envisioned and included. The value of subscript B is dependent upon the element X. The combination of silicon substrate and self-assembled monolayer serves as an integrated circuit element.

B. Composition Of Barrier Layer

[17] The diffusion barrier layer includes a self-assembled monolayer. As the term is applied to the present invention, a "self-assembled monolayer" is a single layer of molecules that forms on a substrate surface when monolayer subunits are contacted with the surface under appropriate reaction conditions. The subunits are attached to the substrate at a first end; the second end of the molecule projects upward from the substrate surface. As surface sites on the surface are reacted with monolayer subunits, the single molecular layer is formed.

[18] The subunits of the self-assembled monolayer are preferably attached to the substrate through a covalent bond. Typically, the substrate has reactive moieties extending from its surface (*e.g.*, O, OH, NH_2, SH). The reactive moieties provide a point of covalent attachment to the subunit. For instance, SiO_2 is a typical substrate for monolayer formation. The hydroxylated SiO_2 surface provides OH groups that can covalently bind to substrates containing certain types of functional groups.

[19] The first end of the self-assembled monolayer subunit typically includes a silicon atom to which three displaceable groups are attached. The second end typically includes a chemical group primarily composed of carbon. A preferred subunit is shown below (1):



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Y is typically an O-alkyl group (e.g., OCH_3 or OC_2H_5) but can also be other displaceable groups such as Cl. R^2 is an alkyl group, heteroalkyl group, aryl group or heteroaryl group.

[20] "Alkyl group" refers to a straight-chain, branched or cyclic group containing a carbon backbone and hydrogen. Examples of straight-chain alkyl groups include methyl, ethyl, propyl, butyl, pentyl and hexyl. Examples of branched alkyl groups include *i*-propyl, *sec*-butyl and *t*-butyl. Examples of cyclic alkyl groups include cyclobutyl, cyclopentyl and cyclohexyl.

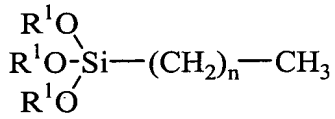
[21] Alkyl groups are substituted or unsubstituted. In a substituted alkyl group, a hydrogen on the carbon backbone is replaced by a different type of atom (*e.g.*, oxygen, nitrogen, sulfur, halogen). For instance, 2-hydroxyethyl is an ethyl group where one of the hydrogens is replaced by an OH group; 2-chloropropyl is a propyl group where one of the hydrogens is replaced by a Cl group.

[22] "Heteroalkyl group" refers to a straight-chain, branched or cyclic group containing a carbon-heteroatom backbone and hydrogen. Heteroatoms include, without limitation, oxygen, nitrogen and sulfur. Methyl ethylether (*i.e.*, $CH_2OCH_2CH_3$) is an example of a straight-chain heteroalkyl group. As with alkyl groups, heteroalkyl groups are substituted or unsubstituted.

[23] "Aryl group" refers to a carbocyclic aromatic group containing six carbon atoms (*e.g.*, phenyl) or a carbocyclic aromatic group containing ten carbon atoms (*e.g.*, naphthyl). An aryl group is substituted or unsubstituted. A substituted aryl group is one where at least one hydrogen atom of an aryl group has been replaced with a different type of atom (*e.g.*, oxygen, nitrogen, sulfur, halogen). Examples of substituted aryl groups include the following: 2-chlorophenyl; 3-methylphenyl; and, 4 methoxyphenyl.

[24] "Heteroaryl group" refers to an aromatic group containing both carbon atoms and heteroatoms. Examples of heteroaryl groups include pyridyl, furyl, pyrrolyl and imidazolyl. As with aryl groups, heteroaryl groups are substituted or unsubstituted. 2-Chloropyridyl is an example of a substituted heteroaryl group.

[25] In one embodiment, the subunit is as shown in structure **2** (R^2 in structure **1** is a straight-chain alkyl):



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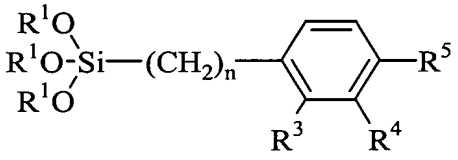
wherein R^1 is a straight-chain alkyl group and n is an integer ≥ 1. Preferably n is an integer ranging from 1 to 5. Preferably, R^1 is methyl and n is 2.

[26] In another embodiment, the subunit is as shown in structure **3** (R^2 in structure **1** is a substituted straight-chain alkyl):



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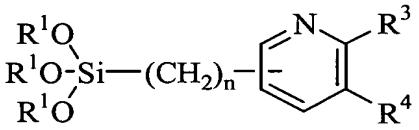
wherein R^1 is a straight-chain alkyl group, n is an integer ≥ 1 and R^3, R^4 and R^5 are independently selected from the group consisting of hydrogen, alkyl groups, heteroalkyl groups, Br, Cl, F, I, NH_2, NHR^6, NR^6R^7, OH, OR^6, SH, SR^6, CHO, COOH and CN. R^6 and R^7 are alkyl groups or aryl groups. Preferably, n is an integer ranging from 1 to 5. Preferably, R^1 is methyl, R^3, R^4 and R^5 are hydrogen and n is 2.

[27] In another embodiment, the subunit is shown in structure **4** (R^2 in structure **1** is a substituted straight-chain alkyl):



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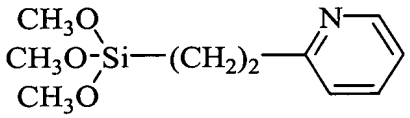
wherein R^1 is a straight-chain alkyl group, n is an integer ≥ 1 and R^3 and R^4 are independently selected from the group consisting of hydrogen, alkyl groups, heteroalkyl groups, Br, Cl, F, I, NH_2, NHR^6, NR^6R^7, OH, OR^6, SH, SR^6, CHO, COOH and CN. R^6 and

R^7 are alkyl groups or aryl groups. Preferably n is an integer ranging from 1 to 5. Preferably, R^1 is methyl, R^3, R^4 and R^5 are hydrogen and n is 2.

[28] A preferred subunit of structure **4** is compound **5**, shown below:



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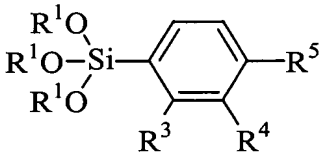
In another embodiment, the subunit is shown in structure **6** (R^2 in structure **1** is an aryl):



6

wherein R^1 is a straight-chain alkyl group, and R^3, R^4 and R^5 are independently selected from the group consisting of hydrogen, alkyl groups, heteroalkyl groups, Br, Cl, F, I, NH_2, NHR^6, NR^6R^7, OH, OR^6, SH, SR^6, CHO, COOH and CN. R^6 and R^7 are alkyl groups or aryl groups.

C. Process For Forming Barrier Layer

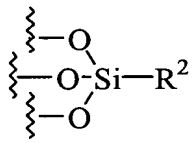
[29] To form the self-assembled monolayer on the surface of a substrate, a substrate is first prepared. The substrate is typically cleaned, washed and dried. Contact of the prepared substrate with monolayer subunits in a suitable solvent and under appropriate reaction conditions attaches the subunits to the surface. Removal of the solvent provides the desired layer on the substrate.

[30] In one embodiment, the substrate is a silicon wafer that has been oxidized to form an SiO_2 surface layer. The layer is typically cleaned using an organic solvent (*e.g.*, xylene) or a series of organic solvents followed by a water wash. The wet wafer is dried, for example, by blow-drying it with N_2. Immersion of the dry wafer in an organic solvent (*e.g.*, toluene) containing self-assembled monolayer subunits followed by heating the solution attaches subunits to the SiO_2 surface. The reacted substrate is washed with an organic solvent (e.g., toluene) and dried (*e.g.*, blown dry with N_2).

D. Barrier Layer As Part Of Device

[31] The present invention provides an integrated circuit comprising a self-assembled monolayer diffusion barrier. FIG. 1 shows an MOS test structure containing a self-assembled monolayer barrier layer. The MOS test structure contains the following elements: a silicon layer (1); a silicon dioxide layer (2) on the top side of the silicon layer; an aluminum back contact (3) on the bottom side of the silicon layer; a diffusion barrier (4) comprising a self-assembled monolayer; and, copper dots (5) deposited on the diffusion barrier. FIG. 3 shows a cross-sectional view of a two-level integrated circuit comprising a self-assembled monolayer diffusion barrier layer. The illustrated integrated circuit contains the following elements: a copper layer (6); a self-assembled monolayer diffusion barrier layer (7) that surrounds the copper layer; and, a silicon substrate (8) that includes the copper and diffusion barrier layers.

[32] The self-assembled monolayer in the integrated circuit is composed of subunits. Where the subunits are covalently attached to a substrate surface, one representation of such a subunit is shown below (**7**, wavy lines represent covalent attachment to the substrate):



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wherein R^2 is an alkyl group, heteroalkyl group, aryl group or heteroaryl group.

E. Metals Deposited On Diffusion Barrier

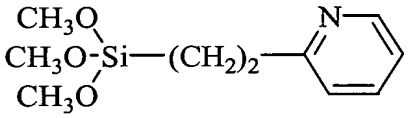
[33] The diffusion barrier of the present invention serves to inhibit the diffusion of a deposited metal on the surface of the self-assembled monolayer through to the substrate underneath the monolayer. The barrier inhibits the diffusion of a variety of metals. In a preferred embodiment, the barrier inhibits the diffusion of copper.

F. Examples

1. Preparation Of An MOS Test Structure.

[34] A (100) oriented, B-doped, 5" diameter p-Si wafer was taken. It was RCA cleaned and oxidized in an ambient of dry O_2 at 900 °C to grow an oxide of 100 nm thickness. The back oxide was completely removed using buffered HF and a 0.3 – 0.4 μm-thick aluminum layer was sputter deposited to form a back contact. The resulting wafer was vacuum annealed at 400 °C for 30 minutes.

[35] The vacuum annealed wafer was respectively cleaned in xylene, acetone and isopropyl alcohol followed by a thorough deionized water wash. The washed wafers were blown dry with N_2 and immersed in a 1% (by volume) solution of organosilane (*i.e.*, self-assembled monolayer subunit) in toluene. The following subunits (purchased from Gelest Inc. of Tullytown, Pennsylvania) were used in the process:



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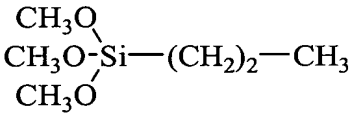

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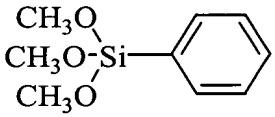

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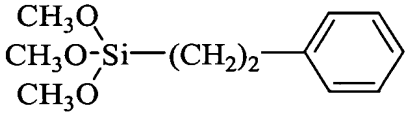

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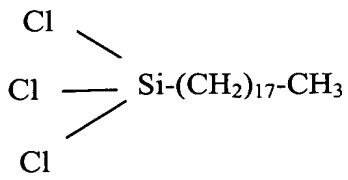

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[36] The wafer in the solution was heated from room temperature to 60 °C over 1 hour. The wafer was washed with toluene, blown dry with N_2 and baked on a heating plate for about 4 minutes at 120 °C.

[37] Copper dots of 1 mm diameter and 1.2 μm thickness were sputter deposited on the wafer monolayer, completing the preparation of the MOS test structure.

2. Bias Temperature Testing Of MOS Test Structures

[38] Test structures prepared according to Example 1 were subjected to electrical testing. A control structure (no diffusion barrier) and four different structures comprising self-assembled monolayer diffusion barriers (diffusion barrier comprising subunits **5**, **8**, **9** and **10** respectively) were biased at 2 MV/cm and 200 °C for 30 minutes in nitrogen ambient. Failure of each respective specimen was recorded. FIG. 2 shows a bar graph representing several trials of each of the 5 structures and the failure time in minutes for each respective structure.